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Xu Youyun; Li Zongwang; Ruan Ming; Luo Hanwen; Song Wentao;
Electrical and Computer Engineering, 2001. Canadian Conference on
Volume 1, 13-16 May 2001 Page(s):241 - 245 vol.1
Digital Object Identifier 10.1109/CCECE.2001.933690

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☐   2.   **A 3.33Gb/s (1200,720) low-density parity check code decoder**
Chien-Ching Lin; Kai-Li Lin; Hsie-Chia Chang; Chen-Yi Lee;
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12-16 Sept. 2005 Page(s):211 - 214
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☐   3.   **80960-next generation**
Hinton, G.;
COMPCON Spring '89. Thirty-Fourth IEEE Computer Society International Conference: Intellectual
Papers.
27 Feb.-3 March 1989 Page(s):13 - 17
Digital Object Identifier 10.1109/CMPCON.1989.301896

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☐   4.   **A sub-word-parallel Galois field multiply-accumulate unit for digital signal processors**
Roy, S.;
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Digital Object Identifier 10.1109/ISCAS.2005.1464915

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☐   5.   **A highly efficient domain-programmable parallel architecture for iterative LDPCC decoding**
Al-Rawi, G.; Cioffi, J.;
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2-4 April 2001 Page(s):569 - 577
Digital Object Identifier 10.1109/ITCC.2001.918858

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6. **Loosely coupled memory-based decoding architecture for low density parity check codes**
Se-Hyeon Kang; In-Cheol Park;
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8. **Implementation of an LDPC decoder on a vector signal processor**
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Volume 1, 4-7 July 2001 Page(s):34 - 36 vol.1
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Xinjia Chen; Kemin Zhou; Aravena, J.L.;
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Gass, W.;
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